**Muhammad Azri bin Zainuddin WER150018**

**Tutorial 3**

**Question 3**

**Full Adder**

library ieee;

use ieee.std\_logic\_1164.all;

entity adder1 is

port (

a, b, cin: in std\_logic;

s, cout: out std\_logic

);

end adder1;

architecture add of adder1 is

signal s0, s1, s2: std\_logic;

begin

s0 <= a XOR b;

s1 <= cin AND s0;

s2 <= a AND b;

s <= s0 XOR cin;

cout <= s1 OR s2;

end add;

**4-bit Full Adder**

library ieee;

use ieee.std\_logic\_1164.all;

entity fulladder is

port (

a: in std\_logic\_vector(3 downto 0);

b: in std\_logic\_vector(3 downto 0);

cin: in std\_logic;

sum: out std\_logic\_vector(3 downto 0);

c\_out: out std\_logic

);

end fulladder;

architecture fulladd of fulladder is

component adder1 is

port (

a, b, cin: in std\_logic;

s, cout: out std\_logic

);

end component;

signal s: std\_logic\_vector(2 downto 0);

begin

fa0: adder1 port map (a=>a(0), b=>b(0), cin=>cin, cout=>s(0), s=>sum(0));

fa1: adder1 port map (a=>a(1), b=>b(1), cin=>s(0), cout=>s(1), s=>sum(1));

fa2: adder1 port map (a=>a(2), b=>b(2), cin=>s(1), cout=>s(2), s=>sum(2));

fa3: adder1 port map (a=>a(3), b=>b(3), cin=>s(2), cout=>c\_out, s=>sum(3));

end fulladd;



